Remarks on Reversible Circuit Synthesis from Decision Diagrams

An Informal Research Group

Suzana Stojković
Milena Stanković
Radomir S. Stanković

University of Niš, Faculty of Electronic Engineering

Claudio Moraga

technische universität dortmund

Decision Diagrams

Data structure for representation of discrete functions

Directed acyclic graph consisting of a set of non-terminal nodes and constant nodes connected with edges

Graphic representation of function expressions for discrete functions

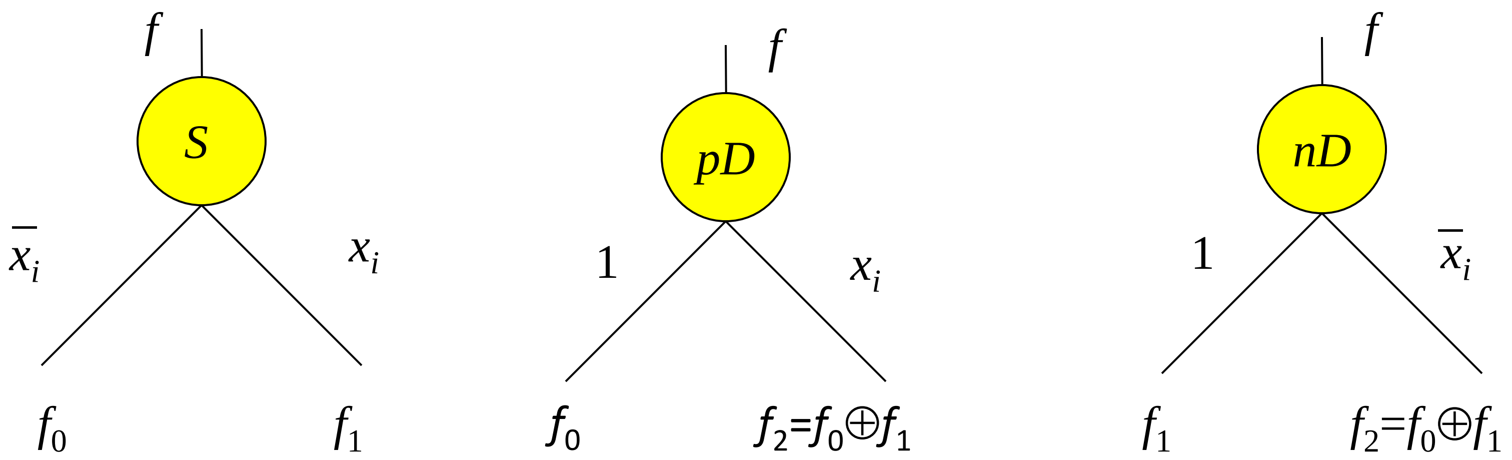
Binary Decision Diagrams

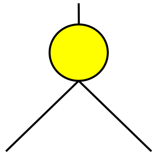
S - node $\quad f = \bar{x}_i f_0 \oplus x_i f_1$

pD - node $\quad f = 1 \cdot f_0 \oplus x_i (f_0 \oplus f_1)$

nD - node $\quad f = 1 \cdot f_1 \oplus \bar{x}_i (f_0 \oplus f_1)$

Bit-level diagrams

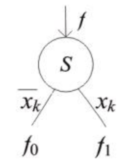
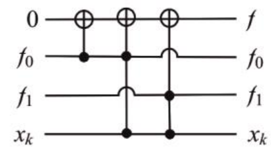
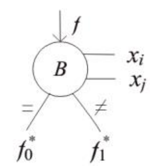
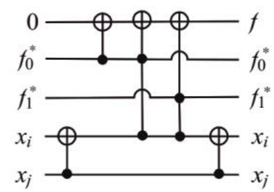
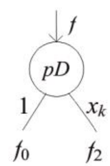
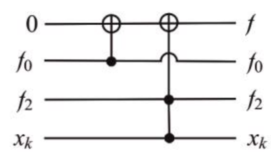
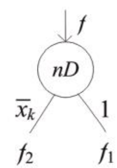
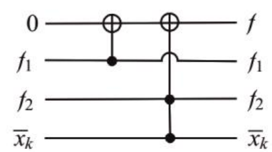




$\in \{S, pD, nD\}$ by level → Kronecker DD

pD – nodes FDD (pD,nD) – nodes FPFDD

Realization of BDD, BBDD, and FDD

Diagram Decomposition rule	Node	Realization by Toffoli gates	*QC*
BDD $f = \overline{x}_k f_0 \oplus x_k f_1$			11
BBDD $f = (\overline{x_i \oplus x_j}) f_0^* \oplus (x_i \oplus x_j) f_1^*$			13
Positive Davio $f = f_0 \oplus x_k f_2$			6
Negative Davio $f = f_1 \oplus \overline{x}_k f_2$			6

Reduced number of nodes
Increased cost of a node

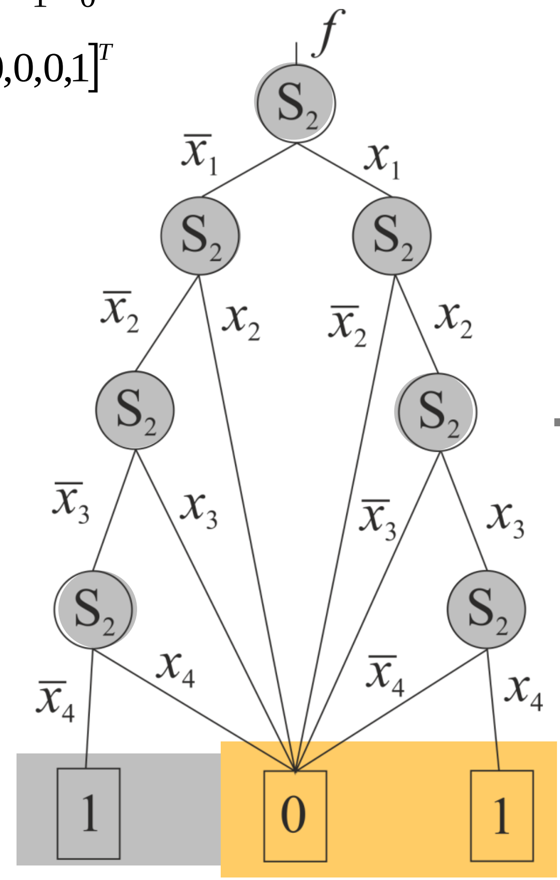
FDD - small cost of a node

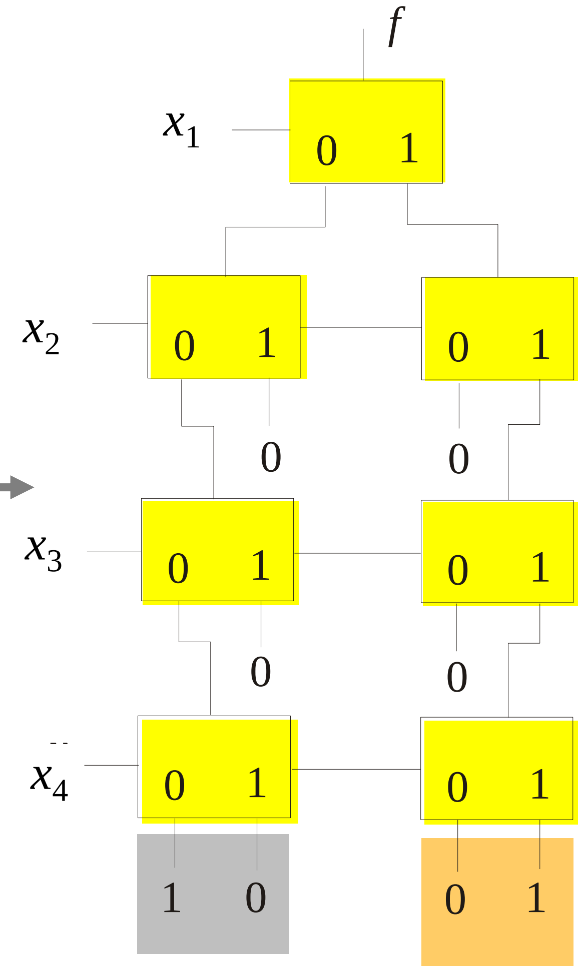
FPDD - reduced number of nodes with small cost of a node

Network from BDD

$$f = \bar{x}_3\bar{x}_2\bar{x}_1\bar{x}_0 + x_3x_2x_1x_0$$

$$\mathbf{F} = [1,0,0,0,0,0,0,0,0,0,0,0,0,0,0,1]^T$$



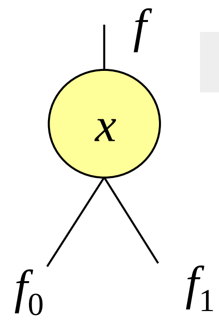


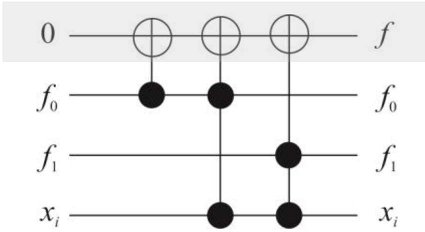
Reversible Circuit Synthesis

Cascade → Tree converted into a linear structure

Traverse the decision diagram
(bottom-up and post-order)

Replace each non-terminal node by
a reversible circuit realizing
the decomposition rule in the diagram



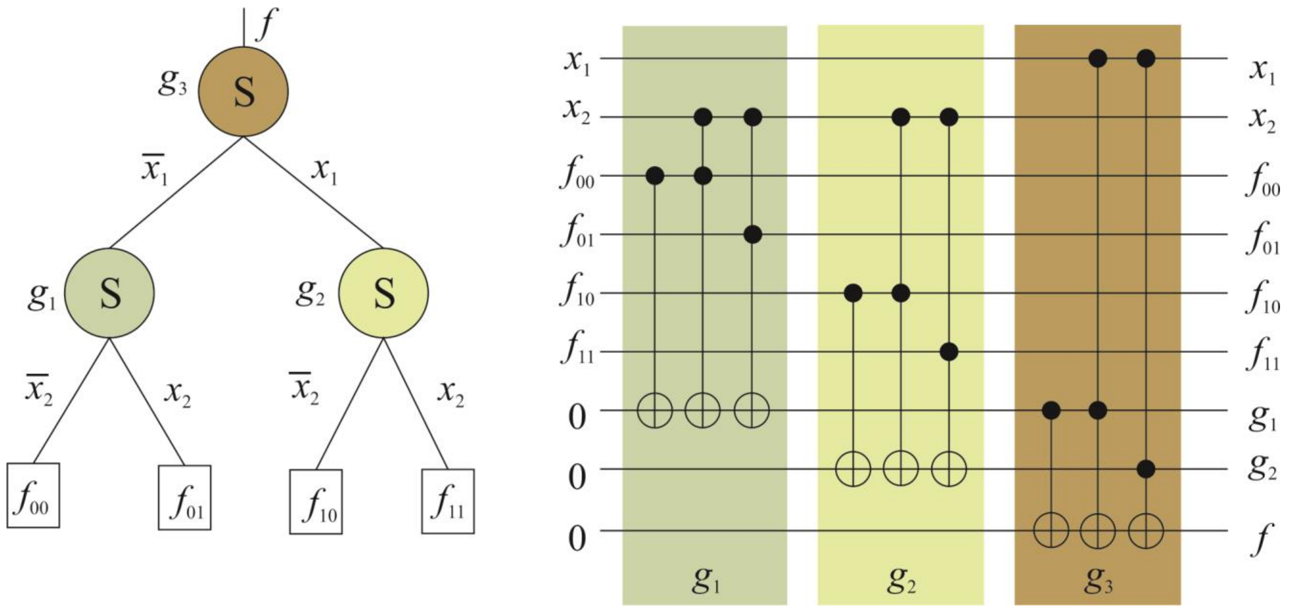


$$f = \bar{x}_i f_0 \oplus x_i f_1 = (1 \oplus x_i) f_0 \oplus x_i f_1 = f_0 \oplus x_i f_0 \oplus x_i f_1$$

Preserve all the input lines and constant nodes for
the usage in next levels in the cascade

Main drawback – large number of lines

Reversible Circuit from BDD



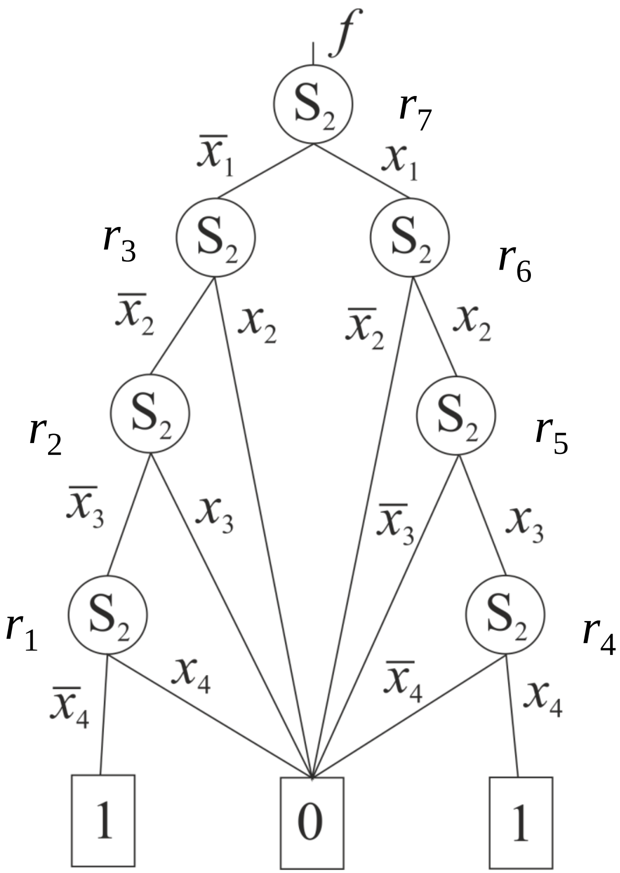
$$g_1 = \overline{x}_2 f_{00} \oplus x_2 f_{01} = f_{00} \oplus x_2 f_{00} \oplus x_2 f_{01}$$

$$g_2 = \overline{x}_2 f_{10} \oplus x_2 f_{11} = f_{10} \oplus x_2 f_{10} \oplus x_2 f_{11}$$

$$g_3 = \overline{x}_1 g_1 \oplus x_1 g_2 = g_1 \oplus x_1 g_1 \oplus x_1 g_2$$

Reversible Circuit from BDD

$f = \bar{x}_3\bar{x}_2\bar{x}_1\bar{x}_0 + x_3x_2x_1x_0$ $\mathbf{F} = [1,0,0,0,0,0,0,0,0,0,0,0,0,0,0,1]^T$

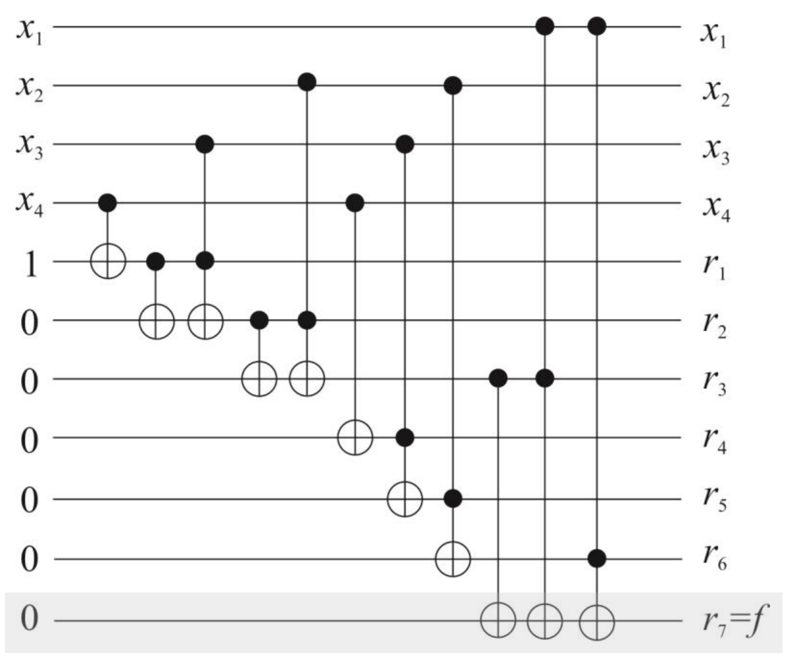


$r_1 = \bar{x}_4 = 1 \oplus x_4$ $r_4 = x_4$

$r_2 = \bar{x}_3 = r_1 \oplus x_3 r_1$ $r_5 = x_3 \cdot r_4$

$r_3 = \bar{x}_2 \cdot r_2 = r_2 \oplus x_2 r_2$ $r_6 = x_2 \cdot r_5$

$r_7 = \bar{x}_1 \cdot r_3 \oplus x_1 r_6 = r_3 \oplus x_1 r_3 \oplus x_1 r_6$



Optimization Possibilities

Decision diagrams defined with respect to
different decomposition rules

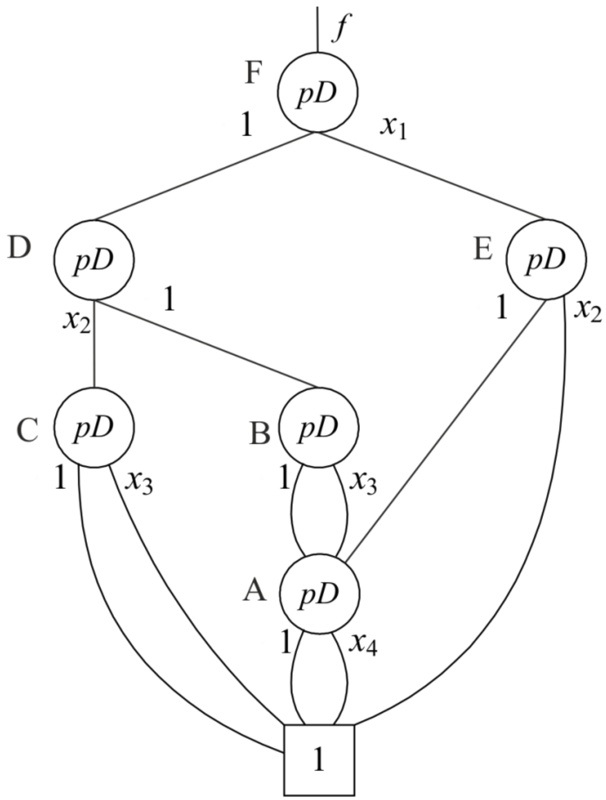
Reduce diagrams from the selected class by different methods

Variable ordering
Linearization of variables
Change of the underlying algebraic structure

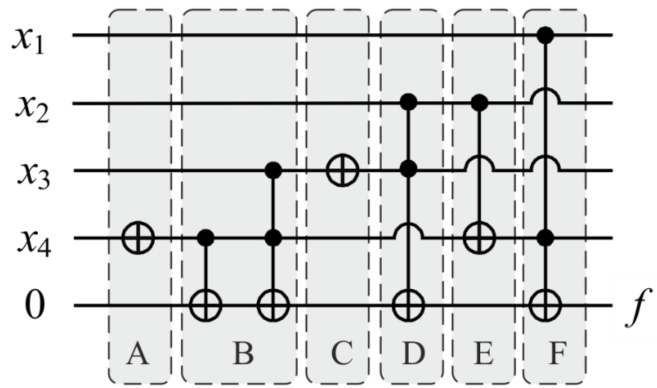
Template based post-processing

FDD – *4mod5_8*

F = [1,0,0,0,0,1,0,0,0,0,1,0,0,0,0,1]^T **S**$_f$=[1,1,1,1,1,0,1,0,1,1,0,0,1,0,0,0]^T

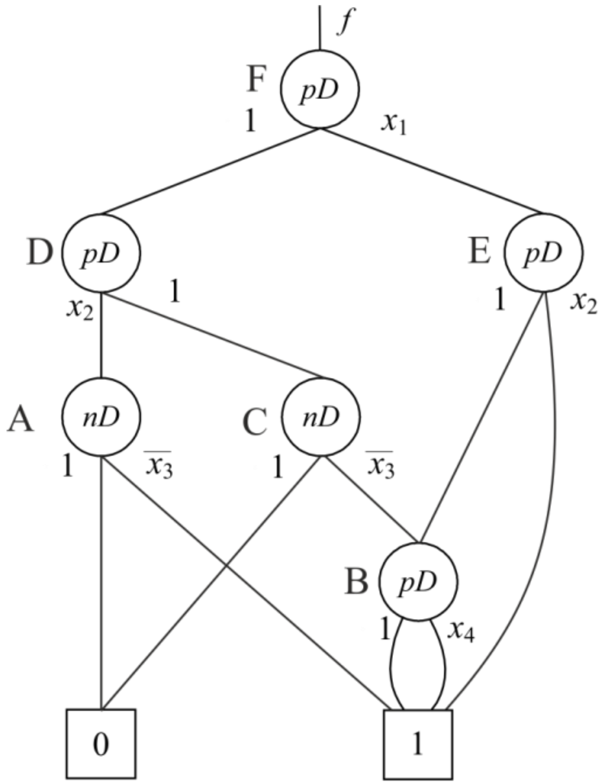


FDD



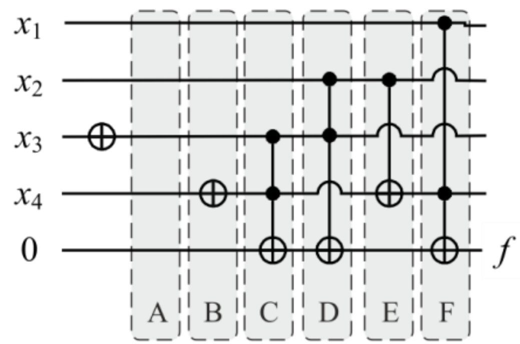
FPFDD – *4mod5_8*

$F = [1,0,0,0,0,1,0,0,0,0,1,0,0,0,0,1]^T$ $\mathbf{S}_f=[0,0,1,1,0,0,1,0,1,1,0,0,1,0,0,0]^T$



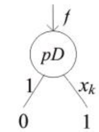
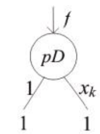
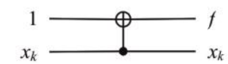
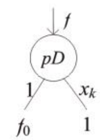
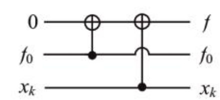
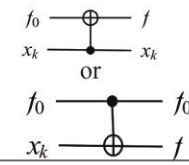
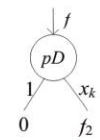
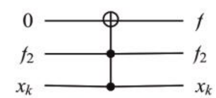
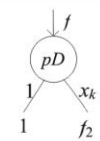
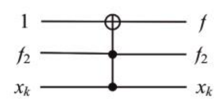
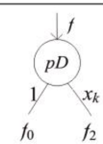
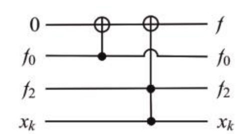
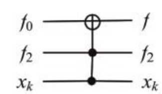
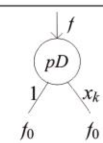
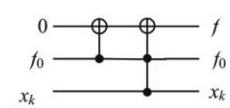
FPFDD

Toffoli gates



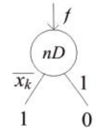
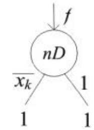
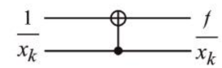
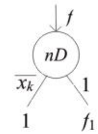
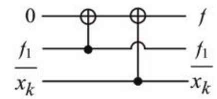
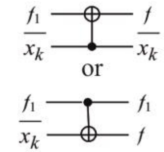
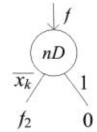
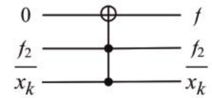
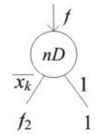
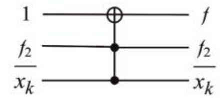
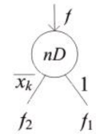
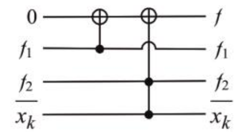
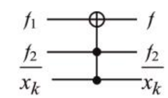
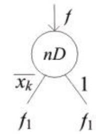
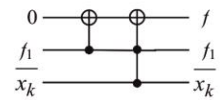
Optimization Possibilities

Positive Davio nodes

Node in FDD	Realization by Toffoli gates	Simplified realization	Condition for simplification
			
			The last usage of line x_k
			The last usage of line f_0 The last usage of line x_k
			
			
			The last usage of line f_0
			

Optimization Possibilities

Negative Davio nodes

Node in FDD	Realization by Toffoli gates	Simplified realization	Condition for simplification
			
			The last usage of line x_k
			The last usage of line f_1 The last usage of line x_k
			
			
			The last usage of line f_1
			

Main Contribution and Present Work

Matching of decision diagrams (decomposition rules) with circuit modules provides networks of smaller cost

Realization of reversible ciruits through Walsh decision diagrams (WDD) and Hadamard modules

Concluding Remarks

Decision diagrams are a suitable data structure for the desing of reversible circuits

Main drawback – a large number of additional lines

Just a few additional lines in the case of FDDs

Optimization possiblities -
Selecting different decision diagrams

Apply methods for further reducing the selected diagrams

Match the diagrams (decomposition rules) with reversible gates to realize nodes